

Appl. No. 10/711,066  
Amdt. dated June 30, 2008  
Reply to Office action of March 31, 2008

**Amendments to the Drawings:**

Please replace Figures 1, 3, and 5 with the attached replacement sheets, respectively.

Attachment:	Replacement Sheet	3 pages
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**REMARKS/ARGUMENTS**

**Figure 1 should be designated by a legend such as –Prior Art—because only that which is old is illustrated.**

Applicant has included a replacement sheet for **Figure 1** having the legend “Prior Art”, as was requested by the Examiner. No new matter is entered.

Additionally, applicant has provided replacement sheets correcting the misspelled word “Decrypt” in both Figures 3 and 5. No new matter is entered.

**Claims 1-2, 5-7, and 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant’s admitted prior art (herein referred to as AAPA) in view of Ishikawa (EP 0440243A2).**

Applicant respectfully disagrees with the Examiner’s rejection of claim 1 as being obvious under 35 U.S.C. 103(a). The applicant first notes that Ishikawa teaches using a microprocessor to drive a memory controller to directly access stored data. What distinguishes applicant’s invention as claimed in claim 1 is that the present invention skips the step of using a direct memory controller. Additionally, Ishikawa accesses a disk and does not involve encrypted data. Applicant’s invention solves the problem of decrypted data getting accessed, saves chip area, and reduces manufacturing cost and circuit complexity.

For at least the above reasons, applicant asserts that claim 1 of the present invention should be found allowable with respect to the teachings of the AAPA with respect to the Ishikawa. Reconsideration of claim 1 is respectfully requested. Claims 2-6 are dependent upon claim 1 and should be found allowable for at least the same reasons. Further comments regarding particular dependent claims are provided in the below paragraphs.

Claim 2 discloses using a register module to store an encrypted instruction. This is not the same as the cache in Ishikawa. In applicant’s disclosure, the encrypted data can also be immediately transmitted to the decryption module to immediately generate the corresponding decrypted instruction. Applicant notes that this is different than a cache

memory.

Concerning claim 5, applicant respectfully disagrees that the further limitation to locate the instruction access controller and the microprocessor on a chip would have been obvious to a person having ordinary skill in the art. In the Office action of 03/31/2008, the Examiner stated that a person of ordinary skill in the art would be able to deduce the present invention as claimed in claim 5 by “merely replacing the DMA controller and memory controller taught by AAPA with an IAC as taught by Ishikawa.” However, the applicant respectfully disagrees and asserts that “[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements...” In re Kuhn, 441 f.3d 977, 988 (CA 10 Fed. 2006)

Concerning claim 6, applicant respectfully asserts that locating the storage apparatus in a chip is not the same as Ishikawa because the storage apparatus includes the encrypted data. The applicant again notes that Ishikawa does not discuss encrypted data. Additionally, locating the storage apparatus on the chip greatly reduces manufacturing cost and circuit complexity.

Concerning independent claim 7, the Examiner stated that **the microprocessor being connected to the decryption module is anticipated by applicant’s admitted prior art**, but applicant respectfully disagrees. As is made clear in paragraph 5 and Figure 1 of applicant’s application, the microprocessor in the prior art is connected to the storage module. “The decryption module 24 is electronically connected to the storage apparatus 26. The storage apparatus is electronically connected to the microprocessor 28, so the microprocessor 28 can access the decrypted instructions from the storage apparatus 26 to execute the decrypted instructions.” This is different than is claimed in claim 7.

Then the Examiner uses Ishikawa to show utilizing a microprocessor to drive the instruction access controller to control a storage apparatus to transmit data for access. Applicant respectfully disagrees. Ishikawa shows data transfer between a microprocessor and a disk, using an interface control unit and a cache (Ishikawa Fig. 1). Applicant eliminates a step and receives the data, the decrypted instruction, from the decryption

module. The Examiner says that encrypted data is nothing more than data stored in an external memory, but it is more than that. It is data that must be decrypted, and efficiently. Applicant doesn't simply substitute one known element for another to obtain predictable results. The microprocessor is used to drive the instruction access controller to control the storage module to transmit the encrypted instruction to the decryption module. Thus the probing possibility of decrypted instructions and reducing manufacturing cost and the chip area are reduced.

For at least the above reasons, applicant asserts that claim 7 of the present invention should be found allowable with respect to the teachings of the AAPA with respect to the Ishikawa. Reconsideration of claim 7 is respectfully requested. Claims 8-15 are dependent upon claim 7 and should be found allowable for at least the same reasons. Further comments regarding particular dependent claims are provided in the below paragraphs.

**Claims 3 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (herein referred to as AAPA) in view of Ishikawa (EP 0440243A2) in further view of Kawaguchi (US 7,228,436).**

Claim 3 depends from claim 1, and should be allowed for all the reasons given above for claim 1. Claim 10 depends from claim 7 and should be allowed for all the reasons given above for claim 7, as well as those reasons given for claim 3.

**Claims 4 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (herein referred to as AAPA) in view of Ishikawa (EP 0440243A2) in further view of Lee (US 2004/0177262) and Kawaguchi (US 7,228,436).**

Claim 4 depends from claim 1, and should be allowed for all the reasons given above for claim 1. Applicant also respectfully argues that encrypting the address where the encrypted instructions are located, and then storing a key that has to be read to decrypt the

access address is far from obvious. **Lee encrypts the address, but doesn't use a stored key. Kawaguchi uses a stored key, but doesn't encrypt the address.** Improving similar devices by using known techniques is not the same thing as incorporating Lee and Kawaguchi. Applicant respectfully argues that the Examiner has not provided a sufficient  
5 reason or sufficient analysis of why the disclosures of the references should be combined.

Claim 11 depends from claim 7 and should be allowed for all the reasons given above for claim 7. In addition, claim 11 is substantially similar to claim 4, and should be allowed for all the reasons given above for claim 4.

10 **Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (herein referred to as AAPA) in view of Ishikawa (EP 0440243A2) in further view of Hu (US 6,170,043).**

Claim 8 is dependent on claim 7, and should be allowed for all the reasons given above for claim 7. Applicant also respectfully disagrees with the Examiner's argument  
15 that the firmware update disclosed in Hu FIG. 6-7 is the same as claim 8 of the present application. The fact is nothing in Hu is encrypted. It wouldn't have been obvious to incorporate a firmware update into the encryption method of the present application because using an address stored in a cache to update information is not the same as storing an encrypted instruction in a cache and then transmitting the encrypted instruction  
20 to a decryption module. Transmitting and updating are two different things.

Claim 9 depends from claim 8, and should be allowed for all the reasons given above for claim 8 and for independent claim 7 from which claim 8 depends.

25 **Claims 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (herein referred to as AAPA) in view of Ishikawa (EP 0440243A2) in further view of Takahashi et al (US 5,825,878).**

Claim 13 depends on claim 12, and should be allowed for all the reasons given above for claim 12, and also for claim 7 on which claim 12 depends. In addition,

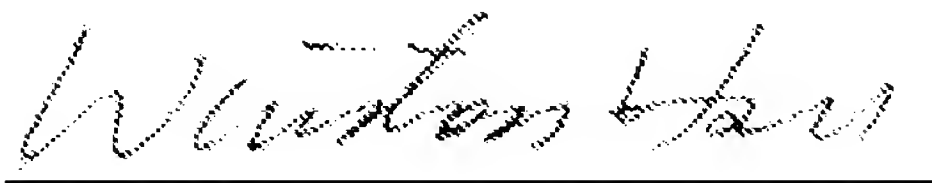
applicant respectfully disagrees that it would have been obvious to a person having ordinary skill in the art to use non-volatile memory as the storage apparatus.

### **Conclusion**

5           Thus, all pending claims are submitted to be in condition for allowance with respect to the cited art for at least the reasons presented above. The Examiner is encouraged to telephone the undersigned if there are informalities that can be resolved in a phone conversation, or if the Examiner has any ideas or suggestions for further advancing the prosecution of this case.

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Sincerely yours,



Date: 06/30/2008

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)